FAIRCHILD SEMICONDUCTOR®

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RMWL38001

37-40 GHz Low Noise Amplifier MMIC

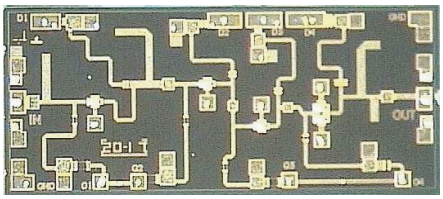
General Description

The RMWL38001 is a 4-stage GaAs MMIC amplifier designed as a 37 to 40 GHz Low Noise Amplifier for use in point to point and point to multi-point radios, and various communications applications. In conjunction with other Fairchild RF Components amplifiers, multipliers and mixers it forms part of a complete 38 GHz transmit/receive chipset. The RMWL38001 utilizes our 0.25µm power PHEMT process and is sufficiently versatile to serve in a variety of low noise amplifier applications.

Features

- 4 mil substrate
- Noise figure 2.7dB (typ.)
- Small-signal gain 22dB (typ.)
- 1 dB compressed Pout 13.5dBm (typ.)
- Chip size 2.9mm x 1.25mm

Device



Absolute Ratings

Symbol	Parameter	Ratings	Units
Vd	Positive DC voltage (+4V Typical)	+6	V
Vg	Negative DC voltage	-2	V
Vdg	Simultaneous (Vd – Vg)	8	V
I_D	Positive DC Current	75	mA
P_{IN}	RF Input Power (from 50 Ω source)	+6	dBm
T_C	Operating Baseplate Temperature	-30 to +85	°C
T_{stg}	Storage Temperature Range	-55 to +125	°C
R_{JC}	Thermal Resistance (Channel to Backside)	169	°C/W

Electrical Characteristics (At 25°C), 50 Ω system, Vd = +4V, Quiescent Current Idq = 50 mA

Parameter	Min	Typ	Max	Units
Frequency Range	37		40	GHz
Gate Supply Voltage (Vg)[1]		-0.5		V
Noise Figure		2.7	4.0	dB
Gain Small Signal at Pin = -20 dBm		22		dB
GainVariation vs Frequency		1.5		dB
Gain at 1 dBm Compression		21		dB
Power Output at 1 dB Compression		13.5		dBm
Power Output Saturated		15		dBm
Drain Current at Pin = -20 dBm		50		mA
Drain Current at 1dB Compression		55		mA
Input Return Loss (Pin = -15 dBm)		12		dB
Output Return Loss (Pin = -15 dBm)		13		dB
OIP3		23		dBm

Note:
1: Typical range of negative gate voltage is -0.9 to -0.1 V to set typical Idq of 50 mA.

Application Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE.

Chip carrier material should be selected to have GaAs compatible thermal coefficient of expansion and high thermal conductivity such as copper molybdenum or copper tungsten. The chip carrier should be machined, finished flat, plated with gold over nickel and should be capable of withstanding 325°C for 15 minutes.

Die attachment should utilize Gold/Tin (80/20) eutectic alloy solder and should avoid hydrogen environment for PHEMT devices. Note that the backside of the chip is gold plated and is used as RF and DC ground.

These GaAs devices should be handled with care and stored in dry nitrogen environment to prevent contamination of bonding surfaces. These are ESD sensitive devices and should be handled with appropriate precaution including the use of wrist grounding straps. All die attach and wire/ribbon bond equipment must be well grounded to prevent static discharges through the device.

Recommended wire bonding uses 3 mils wide and 0.5 mil thick gold ribbon with lengths as short as practical allowing for appropriate stress relief. The RF input and output bonds should be typically 0.012" long corresponding to a typical 2 mil gap between the chip and the substrate material.

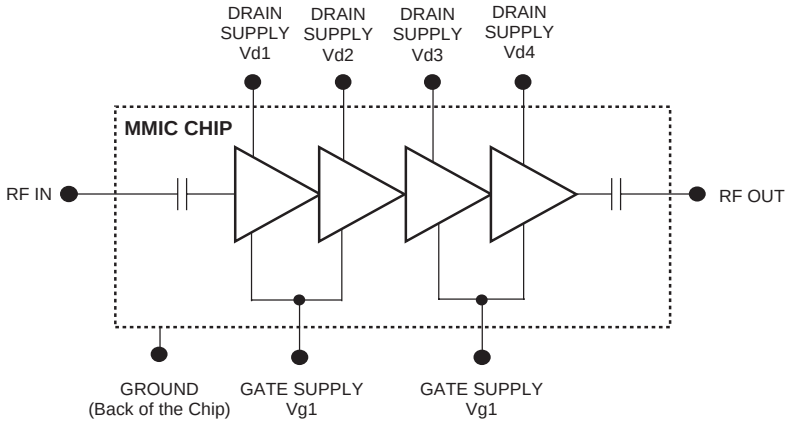
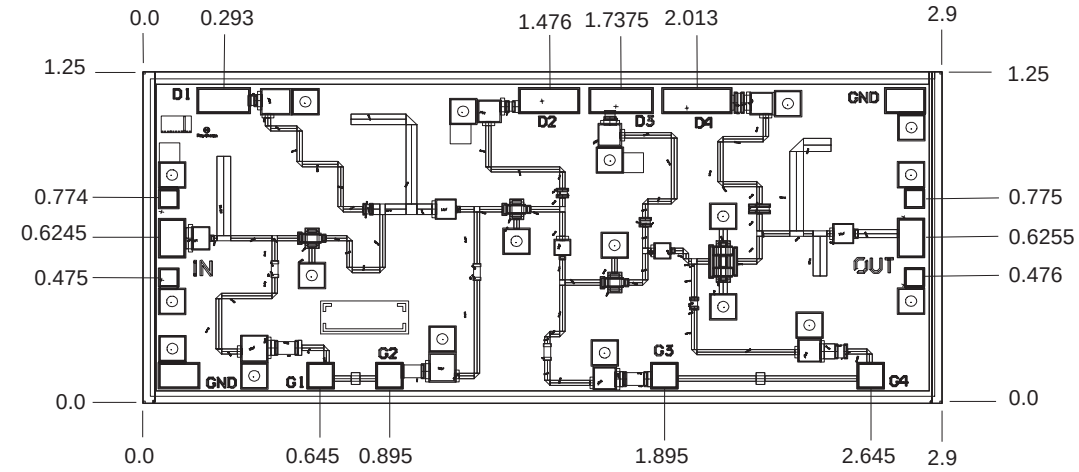


Figure 1. Functional Block Diagram



Dimensions in MM

Figure 2. Chip Layout and Bond Pad Locations
(Chip Size is 2.9mm x 1.25mm x 100µm. Back of chip is RF and DC Ground)

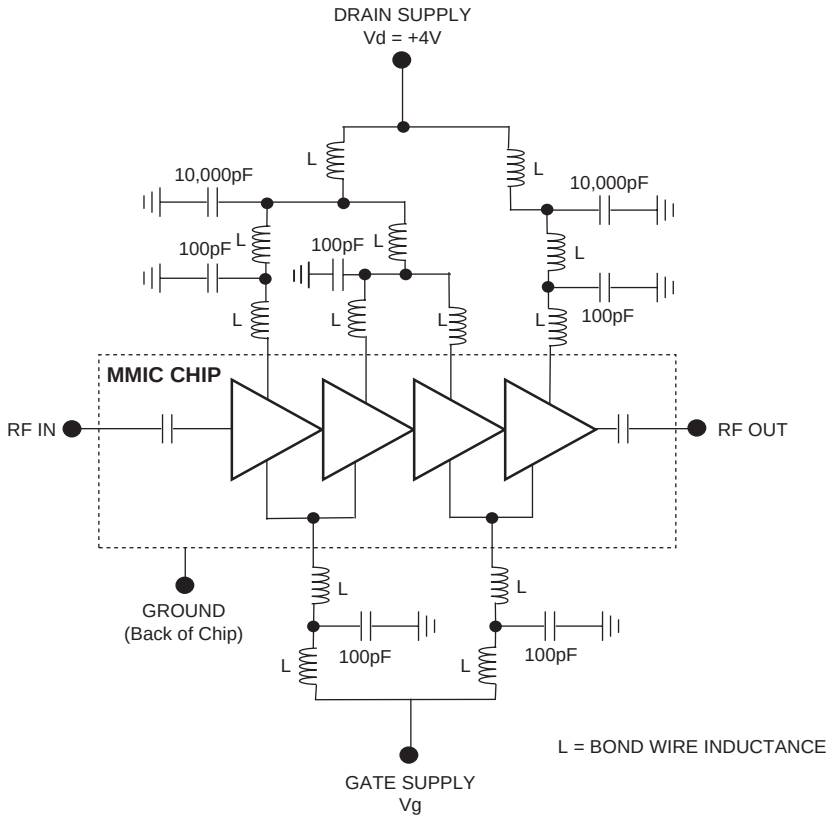
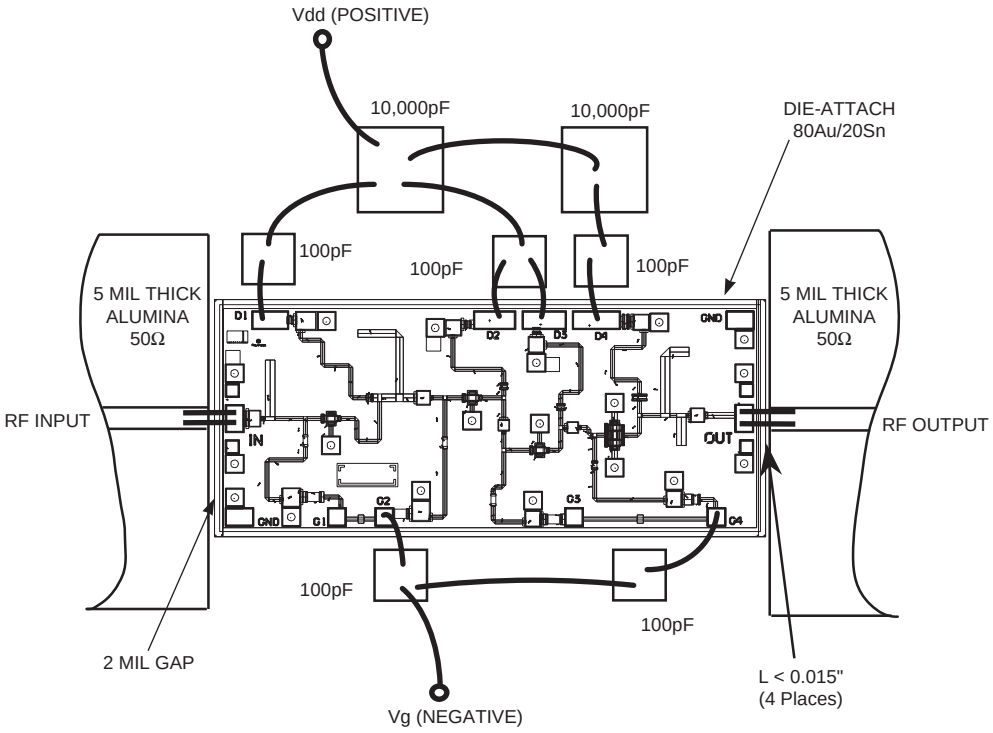


Figure 3. Recommended Application Schematic Circuit Diagram



Note:
Use 0.003" by 0.0005" Gold Ribbon for bonding. RF input and output bonds should be less than 0.015" long with stress relief.

Figure 4. Recommended Assembly Diagram

Recommended Procedure for Biasing and Operation

CAUTION: LOSS OF GATE VOLTAGE (VG) WHILE DRAIN VOLTAGE (VD) IS PRESENT MAY DAMAGE THE AMPLIFIER CHIP.

The following sequence of steps must be followed to properly test the amplifier:

Step 1: Turn off RF input power.

Step 2: Connect the DC supply grounds to the grounds of the chip carrier. Slowly apply negative gate bias supply voltage of -1.5V to Vg.

Step 3: Slowly apply positive drain bias supply voltage of +4V to Vd.

Step 4: Adjust gate bias voltage to set the quiescent current of Idq = 50mA.

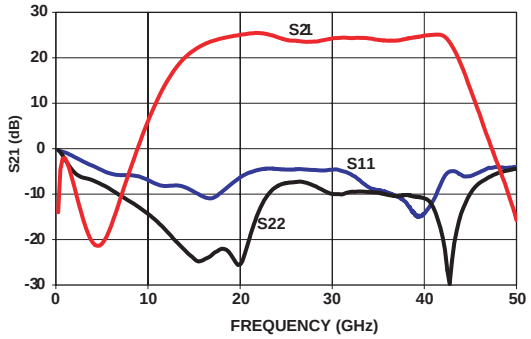
Step 5: After the bias condition is established, RF input signal may now be applied at the appropriate frequency band.

Step 6: Follow turn-off sequence of:

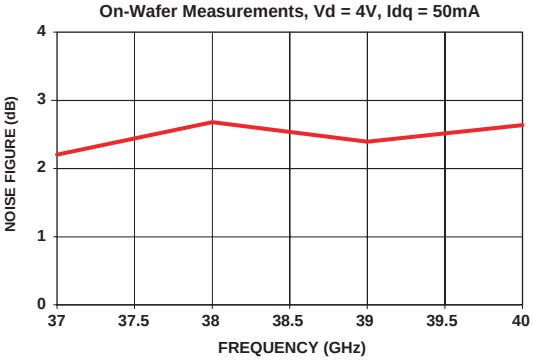
(i) Turn off RF input power,
(ii) Turn down and off drain voltage (Vd),
(iii) Turn down and off gate bias voltage (Vg).

Typical Characteristics

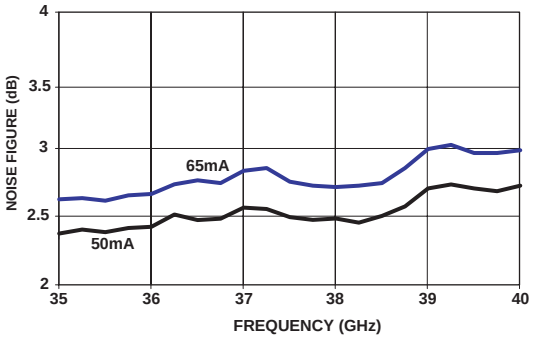
RMWL38001, 37–40GHz Low-Noise Amplifier, Typical Performance, Vd = 4V, Idq = 50mA, Chip Bonded into 50Ω Test Fixture



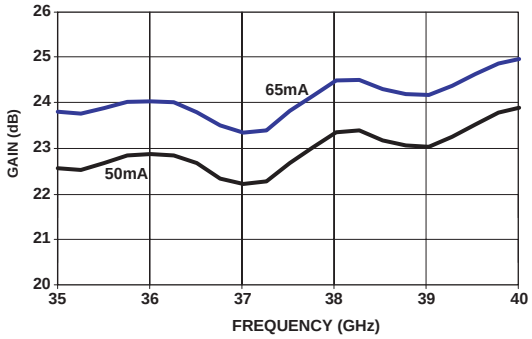
RMWL38001, 37–40GHz Low-Noise Amplifier, Typical Performance, On-Wafer Measurements, Vd = 4V, Idq = 50mA



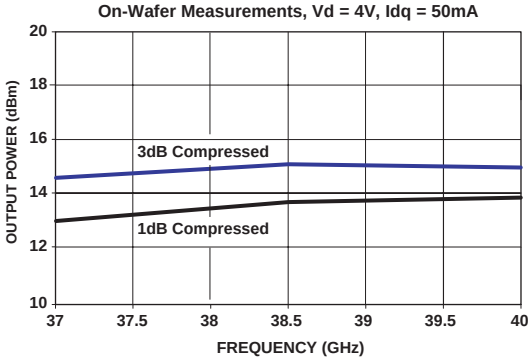
RMWL38001, 37–40GHz Low-Noise Amplifier, Typical Noise Figure, Vd = 4V, Idq = 50mA and 65mA, Chip Bonded into 50Ω Test Fixture



RMWL38001, 37–40GHz Low-Noise Amplifier, Typical Performance, Vd = 4V, Idq = 50mA and 65mA, Chip Bonded into 50Ω Test Fixture



RMWL38001, 37–40GHz Low-Noise Amplifier, Typical Performance, On-Wafer Measurements, Vd = 4V, Idq = 50mA



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CROSSVOLT™	GlobalOptoisolator™	MicroPak™	QS™	SyncFET™
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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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